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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TRINH, MICHAEL MANH	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 10/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/714,207	CHIU ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 5-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 5-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's amendment submitted 3/2/06 and RCE request filed April 04, 2006. Claims 1-2,5-10 are pending. Claims 3-4,11-39 were canceled.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

1. Claims 1,5 are rejected under 35 U.S.C. 102(b) as being anticipated by Yeh et al (6,207,565).

Yeh et al teach an integrated process flow involving a patterned photoresist layer 208 on a substrate 102 in an etching tool that has one or more process chambers, said patterned photoresist layer 208 having an opening with a top and bottom that extends through at least one underlying layer 104 in said substrate 102, comprising: (a) performing an oxygen ashing step to remove said patterned photoresist layer 208 (Figs 9, col 6, lines 47-55; col 2, lines 38-54; col 1, lines 35-53); (b) cleaning a residue from the opening by performing a halogen containing plasma step, in which oxide etch by using a dry plasma etch, such as CF_4, to remove the oxide that grew onto the semiconductor substrate (col 6, lines 56 through col 7; Fig 9; col 2, lines 38-54; col 1, lines 35-53) ; and (c) after dry plasma etch to clean the residues, etching the cleaned opening in the substrate by performing a CF_4/H_2O plasma in the substrate (col 6, line 64 through col 7; Fig 9), wherein, as shown in Figure 6 (Figure 9, col 6, lines 47-67, col 7, col 5, lines 50-67), the steps (a), (b), and (c) are performed in the same process chamber of the etching tool by introducing or stopping of the plasma (see Table I, Figure 6, and col 5, lines 50-67, col 6, lines 47-67) into the inductively-coupled plasma chamber of the Mattson Aspen ashing system. Re claim 5, wherein the halogen containing plasma step involves a plasma of CF_4, CHF_3, C_2F_6, which plasma satisfies $C_xF_yH_z$ where x and y are integers and z is an integer or is 0 (col 6, lines 56-63; col 7, lines 7, lines 22-25).

Claim Rejections - 35 USC § 103

2. Claims 1,5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al (6,025,273) in view of Yeh et al (6,207,565) and Applicant's admitted prior art (present specification page 1).

Chen teaches an integrated process flow involving a patterned photoresist layer 18 on a substrate 12/10 in an etching tool that has one or more process chambers, said patterned photoresist layer 18 having an opening with a top and bottom that extends through at least one underlying layer 16 in said substrate, comprising: (a) performing an oxygen ashing step to remove said patterned photoresist layer 18 (Figs 3-4; col 4, lines 51-65); and (c) etching the opening in the substrate to transfer the opening through an exposed layer at the bottom of the opening in said substrate (Fig 5, col 5, lines 1-20). Re claim 5, wherein said halogen containing plasma step involves a plasma of CF_4, CHF_3, C_2F_6, which plasma satisfies $C_xF_yH_z$, where x and y are integers and z is an integer or is 0 (col 4, lines 64 through col 5, line 5). Chen also teaches (at col 4, lines 55-67) the etching tool including reactive ion etching (RIE) or a HDP etcher.

Re claim 1, Chen lacks cleaning a residue from the opening by performing a halogen containing plasma after oxygen ashing to remove the photoresist layer, and lacks mentioning to perform the steps in the same process chamber of the etching tool.

However, Yeh teaches (at col 6, lines 38 through col 7; Fig 9; col 2, lines 38-54; col 1, lines 35-53) cleaning to remove residues from the opening by performing a halogen containing plasma after oxygen ashing to remove the photoresist layer, since residues are existed on the substrate. Yeh also teaches, at Table I of Figure 6 (Figure 9, col 6, lines 47-67, col 7, col 5, lines 50-67), the steps (a), (b), and (c) are performed in the same process chamber of the etching tool by introducing or stopping of the plasma (see Table I, Figure 6) into the inductively-coupled plasma chamber of the Mattson Aspen ashing system. Applicant's admitted prior art teaches (at present specification page 1, last paragraph) to perform the ashing and etching steps in the same process chamber of the etching tool.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to fabricate the semiconductor process flow involving a patterned photoresist layer of Chen by performing a halogen containing plasma to clean and remove residues from the opening after oxygen ashing to remove the photoresist layer, as taught by Yeh. This is because of the desirability to clean and remove residues from the substrate. This is also because of the desirability to prepare a semiconductor substrate which does not allow residues to become trapped on the semiconductor substrate so that other subsequent processes can be surely carried out in a reliable manner, thereby a high quality semiconductor device can be effectively

manufactured. Additionally, it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the steps of oxygen ashing, halogen plasma, and transfer of Chen in the same process chamber of the etching tool. This is at least because of the desirability to reduce production and equipment cost and processing time, since only a tool is needed.

3. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al (6,025,273) and Yeh et al (6,207,565) and Applicant's admitted prior art (present specification page 1), as applied to claims 1,5 above, taken with Shan et al (6,232,236) and Levenson et al (2001/0038089).

The references including Chen and Yeh teach an integrated process flow involving a patterned photoresist layer 18 as applied to claims 1 and 5 above.

Re claim 2, the references including Chen lacks listing etching tool being a split power etcher, a dual power etcher, a single power etch tool, a reactive ion etcher, or a conventional barrel, direct, or downstream type of ashing tool.

However, Shan teaches (at col 5, lines 11-29; col 3, lines 46-55; col 4, lines 15-35) etching tool including a split power etcher, a dual power etcher, a single power etch tool, a reactive ion etcher. Levenson teaches (at col 4, paragraph 46; paragraphs 5-12) plasma ashing tool including down flow, barrel, direct, and downstream type of ashing tool. Chen also teaches (at col 4, lines 55-67) the etching tool including reactive ion etching (RIE) or a HDP etcher.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the oxygen ashing and halogen plasma step of Chen by employing the etching tool of a split power etcher, a dual power etcher, a single power etch tool, a reactive ion etcher, or a barrel, direct, or downstream type of ashing tool, as taught by Shan and Levenson. This is because these tools are alternative and art recognized equivalent tools so that the plasma ashing and etching steps can be effectively performed in a reliable manner.

4. Claim 5-6 are further rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al (6,025,273), Yeh et al (6,207,565) and Applicant's admitted prior art (present specification

page 1), as applied to claims 1,5 above, taken with Hayasaka et al (5,298,112) and Hori et al (5,411,631).

The references including Chen and Yeh teach an integrated process flow involving a patterned photoresist layer 18 as applied to claims 1 and 5 above. Re claims 5-6, Chen already teaches (at col 4, lines 58 through col 5, line 5) halogen containing plasma including Cl_2, HBr, CF_4.

The references including Chen do not list all halogen plasma as recited in claim 5, the plasma includes CF_4, CH_2F_2, SF_6, NF_3, Cl_2 and $C_xF_yH_z$ where x and y are integers and z is an integer or is 0; and Re claim 6, HBr is included in combination with the above halogen plasma.

However, Hori teaches (at col 5, lines 36-54) halogen containing plasma including CF_4, NF3, SF_6, Cl_2, CHF_3, in which $C_xF_yH_z$ where x and y are integers and z is an integer or is 0, wherein HBr is included in combination with the plasma including Cl_2. Chen already teaches (at col 4, lines 58 through col 5, line 5) halogen containing plasma including Cl_2, HBr, CF_4.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the halogen containing plasma step of Chen by employing available known halogen containing plasma including of CF_4, CH_2F_2, SF_6, NF_3, Cl_2 and $C_xF_yH_z$ where x and y are integers and z is an integer or is 0, with HBr included in the halogen plasma, as taught by Hori and Chen. This is because these halogen containing plasma are alternative and art recognized equivalent plasma etchants so that unwanted residues and material can be effectively removed from the substrate in a reliable manner.

5. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al (6,025,273), Yeh et al (6,207,565) and Applicant's admitted prior art (present specification page 1), as applied to claims 1,5 above, taken with Webb et al (5,228,950).

The references including Chen and Yeh teach an integrated process flow involving a patterned photoresist layer 18 as applied to claims 1 and 5 above.

Re claims 7-8, Chen already teaches (at col 4, lines 55-67) using reactive ion etching (RIE) or a HDP etcher for performing the halogen containing plasma step, but lacks detail about process parameters of flow rate, pressure, temperature, power, time period, as recited in claims 7-8.

However, Yeh also teaches (at Fig 6, Table I, Step 2) performing a halogen containing plasma step, with a gas flow rate of about 360 standard cubic centimeters per minute (sccm), a chamber pressure about 0.5 Torr, a chamber temperature of about 250 degree C, a RF power of about 975 Watts, and for a period of less than about 2 seconds. Webb teaches (at col 3, line 9 through col 4, lines 60) performing a NH_3-halogen containing plasma step, with a gas flow rate of about 10-500 standard cubic centimeters per minute (sccm; col 3, lines 23-40), a chamber pressure about 20 milliTorr to about 1Torr (col 3, lines 9-22), a chamber temperature of about 25 to 150 degree C, a RF power ranging of about 50-400 Watts, and for a period of about 5-60 seconds (col 4, lines 1-5, 51-60).

Therefore, the subject matter as a whole would have been obvious to one or ordinary skill in the art at the time the invention was made to select the portion of the prior art's range flow rate, temperature, a RF power ranging for top RF power and bias RF power, pressure, time period, etc., as taught by Yeh and Webb, and known in the art, which is within the range of applicant's claims, because it has been held to be obvious to select a value in a known range by optimization for the best results, and would be an unpatentable modification, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In Re Aller* 104 USPQ 233,255 (CCPA 1955); *In re Waite* 77 USPQ 586 (CCPA 1948); *In Re Swanson* 56 USPQ 372 (CCPA 1942); *In Re Sola* 25 USPQ 433 (CCPA 1935); and *In Re Dreyfus* 24 USPQ 52 (CCPA 1934).

6. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al (6,025,273), Yeh et al (6,207,565) and Applicant's admitted prior art (present specification page 1) , as applied to claims 1,5 above, taken with Verhaverbeke et al (2003/0045098).

The references including Chen and Yeh teach an integrated process flow involving a patterned photoresist layer 18 as applied to claims 1 and 5 above.

The references including Chen already teaches using the patterned photoresist layer 18 during semiconductor fabrication, wherein, the opening exposes an underlying silicon layer 12 and step (c) forms a shallow trench in the silicon layer 12 (Figs 7,5; col 5, lines 1-49).

Chen thus lacks mentioning his method for forming a shallow trench in the substrate (claim 9); and for forming a gate electrode (claim 10).

However, Verhaverbeke teaches (at Figs 16A-16C) applying the method for forming a shallow trench in the substrate (claim 9), wherein the method is also applied (at Figs 15A-15E) for forming a gate electrode (claim 10).

Therefore, it would have been obvious to one or ordinary skill in the art at the time the invention was made to apply the method of Chen for removing residues during the formation of a shallow trench in the substrate and during the formation of a gate electrode, as taught by Verhaverbeke. This is because of the desirability to eliminate unwanted residues from the substrate so that a high quality integrated device can be manufactured in a reliable manner.

Response to Amendment

7. Applicant's remarks filed March 2, 2006 have been fully considered but they are moot in view of the new ground(s) of rejection.

** Applicant remarked (at 3/2/06 remark) that "...the 'Background' section of the patent application is not 'admitted' prior art unless an applicant uses the specific words 'prior art' to expressly state that the information is prior art...MPEP 608.01(c) explains that the 'Background' section of a patent application can include 'prior art or other information'...".

In response, this is noted and found unpersuasive. First, there is no objective evidence in the record presented by Applicant in order to clearly support for applicant's now simply allegation that the "Background" section is not 'admitted' prior art. Second, to the contrary, the "Prior Art" was expressly stated and evidently shown at least in Figure 3 of the present patent application. Accordingly, as a whole, applicant's simply allegation is unfound. Applicant's admitted prior art teaches "...ashing method also enables an integrated etch sequence in which several etch steps including the photresist strip are performed in the same etch chamber or within the same multi-chambered etch tool to increase throughput...".

In any case, especially, as clearly shown in Figure 6 of Yeh, and at col 6, lines 38 through col 7; Fig 9; col 2, lines 38-54; col 1, lines 35-53) the same process chamber (e.g. the inductively-coupled plasma chamber) is used for performing these steps. Indeed, Yeh teaches after performing an OXYGEN PLASMA ASHING to remove the photoresist, performing a HALOGEN PLASMA ETCHING step to clean residue, and performing a PLASMA ETCHING

to the cleaned opening, wherein an inductively-coupled PLASMA chamber are used for ashing and etching. Therefore, the combined references clearly establish a prima facie case of obivouness with reasonable expectation of success to perform and carry out these plasma ashing and plasma etching by using the same plasma chamber. This is because of the desirability to reduce production and equipment cost and processing time, since only a plasma tool is needed.

** Applicant further alleges that "...Applicant's Background mentions performing ashing and etching in the same process chamber, but it does not mention performing a halogen plasma process to clean residue, much less in the same process chamber as the ashing and etching...".

In response, this is noted and found unconvincing. A portion of Applicant's admitted prior art is excerpted herein in that "...ashing method also enables an integrated etch sequence in which several etch steps including the photresist strip are performed in the same etch chamber or within the same multi-chambered etch tool to increase throughput...". Thus, "ashing" step and other "etching" steps can be carried out by using a same chamber. Moreover, in general, ashing, halogen plasma processing to clean residue, and etching the cleaned opening are all considered as etching steps, in which material and/or residue are removed from the substrate.

** Applicant alleges that "...there is no reasonable expectation of success...if it was practical to do so, the entire fabrication of every integrated circuit device would be carried out form start to finish in a single process chamber...".

In response, this is noted and found unconvincing. First, Applicant appears to miss the main point that the combined references prima facie establish and teach at least the claimed invention for performing and carry out these "oxygen plasma ashing" and "plasma etching steps" by using the "same plasma chamber". Second, of course, it is not disagreed that a person skilled in the art would not normallly have any reasonable expectation to perform a mechanical dicing, deposition, laser metlting, bonding, by using the same plasma etching chamber. However, in this case, the combined references clearly establish a prima facie case of obivouness with reasonable expectation of success. Indeed, Chen teaches performing a PLASMA ashing in oxygen to remove the photoresist, and PLASMA etching to etch the contact hole.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 9:00 Am to 5:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The central fax phone number is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Oacs-9

Michael Trinh
Primary Examiner